Discrete LC Delay Line Phasers

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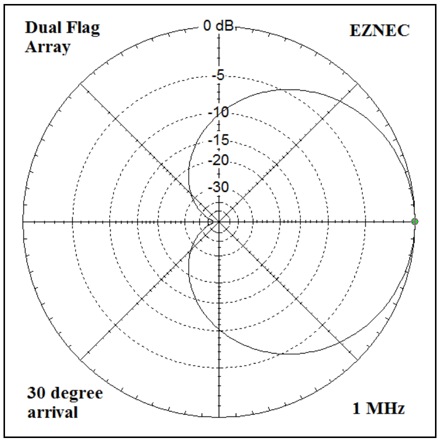
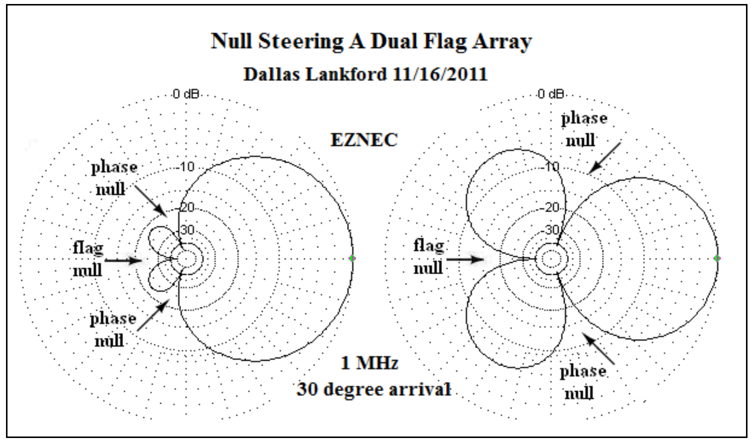
As I said in the articles which developed flag arrays, using a variable phaser with arrays which have very wide 30 dB null apertures is not a good idea because there is no way to adjust the phaser for the widest possible 30 dB null aperture.

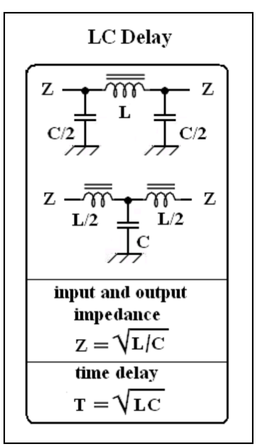




Above left is an EZNEC simulation of an optimal dual flag array with 30 dB null aperture of 90 degrees. Above right are two EZNEC simulations of a dual flag array being null steered with a variable phaser. As the phase nulls (there are two phase nulls) is steered two blips appear on each side of the flag null. The original dual flag array null had a 30 dB null aperture of 90 degrees. As the phase nulls are steered you can clearly see that the apertures of the the null (there are three of them) at 30 dB are much less than 90 degrees. This means that the splatter reduction of a null steered dual flag array is much worse than the splatter reduction of a flag array with a single fixed discrete LC delay line. It does not matter whether a variable delay line phaser, Misek phaser, or some other kind of variable phaser is used to steer the nulls. The result will be the same. It is not a good idea to use a variable phaser and steer nulls for arrays with very wide null apertures.

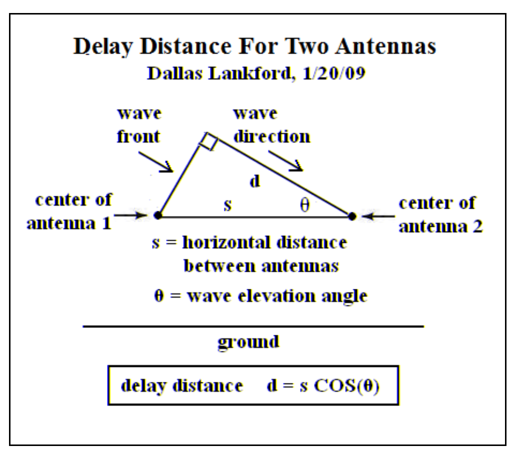
I first came across the schematics and formulas for the π version of discrete LC delay lines during the late 1990's or early 2000's in a data sheet published by Rhombus Industries. Several MW DXers in the USA built phasers using a tapped delay line IC made by Rhombus. The phaser that I built did not work very well (nulls difficult to adjust and not as deep as nulls I could generate with my Misek phaser). From those experiences I concluded that switched delay line phasers were not satisfactory.

Later, in 2009 when I began developing my dual and quad flag antenna arrays, using a single discrete LC delay line phaser turned out to be a very good way to generate the null for those arrays, much better than using coax delay.



The basic discrete LC delay line circuits and formulas are given in the figure at right. I have always used the π circuit instead of the T circuit, but I know of no reason why the T circuit could not be used.

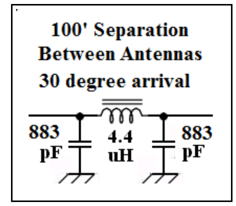
The basic facts about the delay distance between two antennas is given in the figure at left. The delay distance is d = s COS(θ) for an arrival angle θ, where s is the horizontal spacing between the centers of the individual flag antennas. For s = 100', d = 100 COS(30°) = 86.6'. There are 3.28 feet per meter, so d = 86.6/3.28 = 26.4 meters. The angle θ is chosen as 30° for these examples because I have taken 30° as the optimal arrival angle for the very



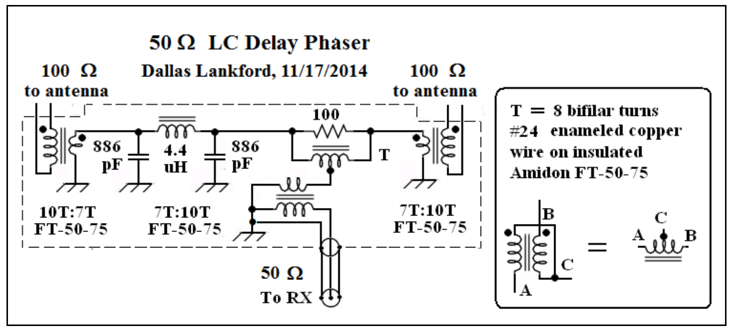
wide 30 dB null apertures of the arrays that I use. Of course, there is no single arrival angle for undesirable signals.

The time delay T is the time difference between the arrival of a wave front at antenna 1 and the arrival of that same wave front at antenna 2. The speed of electromagnetic radiation is approximately 2.99 x 10^8 meters per second in air, so the time delay per meter in air is 1/(2.99 x10^8) = 3.34 nS/m. Thus the time delay T = 3.34 x 26.4 = 88.3 nS.

For a 50 ohm system, take Z = 50 which gives 2500 = L/C, or L = 2500 C. Taking T = 88.3 x 10^–9, which was calculated above (the distance between the centers of the antennas is 100'), both sides of the time formula at right are squared, namely 7796 x 10^–18 = LC, after which substitution of 2500 C for L by the equation above gives 7796 x 10^–18 = 2500 C^2, or C = 1766 pF. Thus C/2 = 883 pF, and L = 2500 x 1766 x 10^–12 = 4.4 µH. The capacitors should be mica, and the inductor may be two series 2.2 µH inductors. In many of the schematics of my other articles the two capacitors of the LC delay circuit are given as 886 pF. I do not know how that happened. The actual capacitance in those circuits (in the circuits I built) was 820//68 = 888 pF. A better choice would be 820//62 = 882 pF. But it hardly matters because the 30 dB null apertures of the flag arrays that I used are so wide.



When I first encountered these discrete LC delay line formulas and circuits, I thought to myself, “Do these really work?” To answer that question I built a discrete LC delay circuit and used it in a dual flag array to see (listen!) if it worked (gave good nulls). I had a very good variable phaser, a variation of a design by Misek, which I had built and which I had used for several years, so I knew what good nulls of my strong MW “clears” to the north should sound like at night. After several nights of listening to my nulled MW clears to the North, I was satisfied that the LC delay phaser worked very well, better, in fact, than the coax delay phaser which I had used at first with my dual flag array. The combiner of this delay line phaser is the balanced transformer T which has been called a magic T combiner. The inputs are the top left and right branches and are 50 ohms. The output at the bottom center is 25 ohms. The magic T combiner impedance values are determined by the value of the resistor, in this case 100 ohms. A 1:2 Z step up transformer is used to match the output to 50 ohms. The two antennas are connected to the phaser with 100 ohm twin lead. The 180 degree phase shift between the antennas is accomplished by the way the antennas are connected to the phaser.

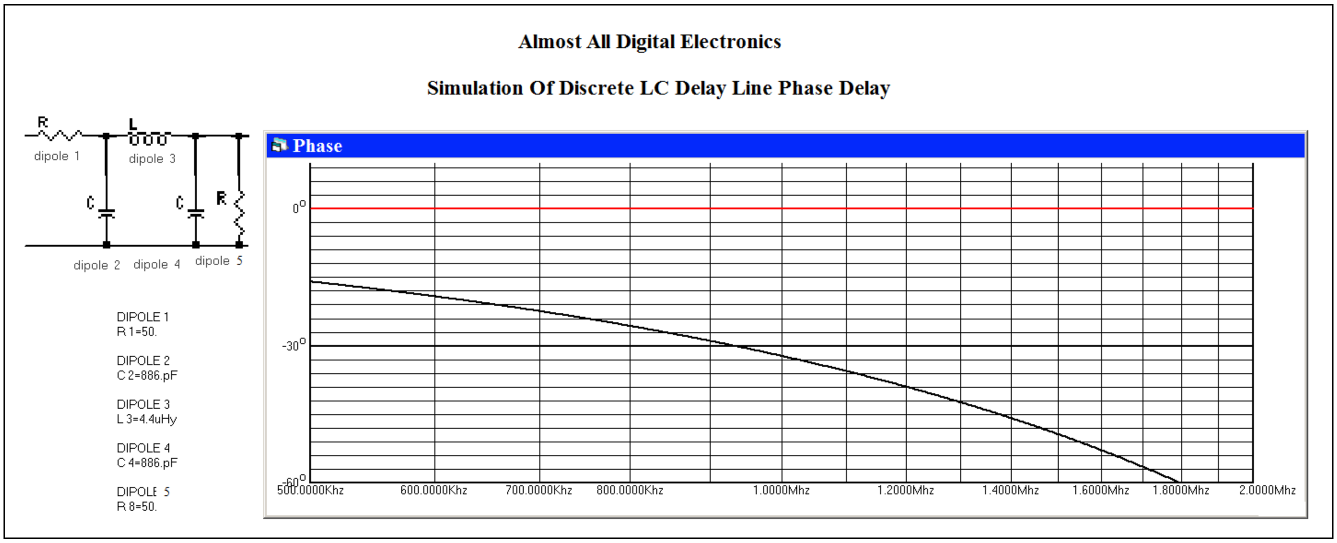


One might ask if the discrete LC delay circuit above gives a uniform 88.3 nS time delay from one end of the MW band to the other. If not, the the nulls would be frequency dependent. Actually, I could tell from the the delay was reasonably uniform because the nulls were so good from one end of the MW band to the other.

However, I wanted another method to evaluate the LC delay phaser. Several years previously I had purchased an inexpensive but excellent inductance (and capacitance and resistance) meter from an on line company called Almost All Digital Electronics (abbreviated AADE) which I used to measure the inductance of inductors that I wound for various purposes. AADE also had free filter simulation software which I had downloaded and installed on my computer. The discrete LC delay circuit resembles a low pass filter, so I used an AADE low pass filter with changed component values to simulate the LC delay circuit phase delay.

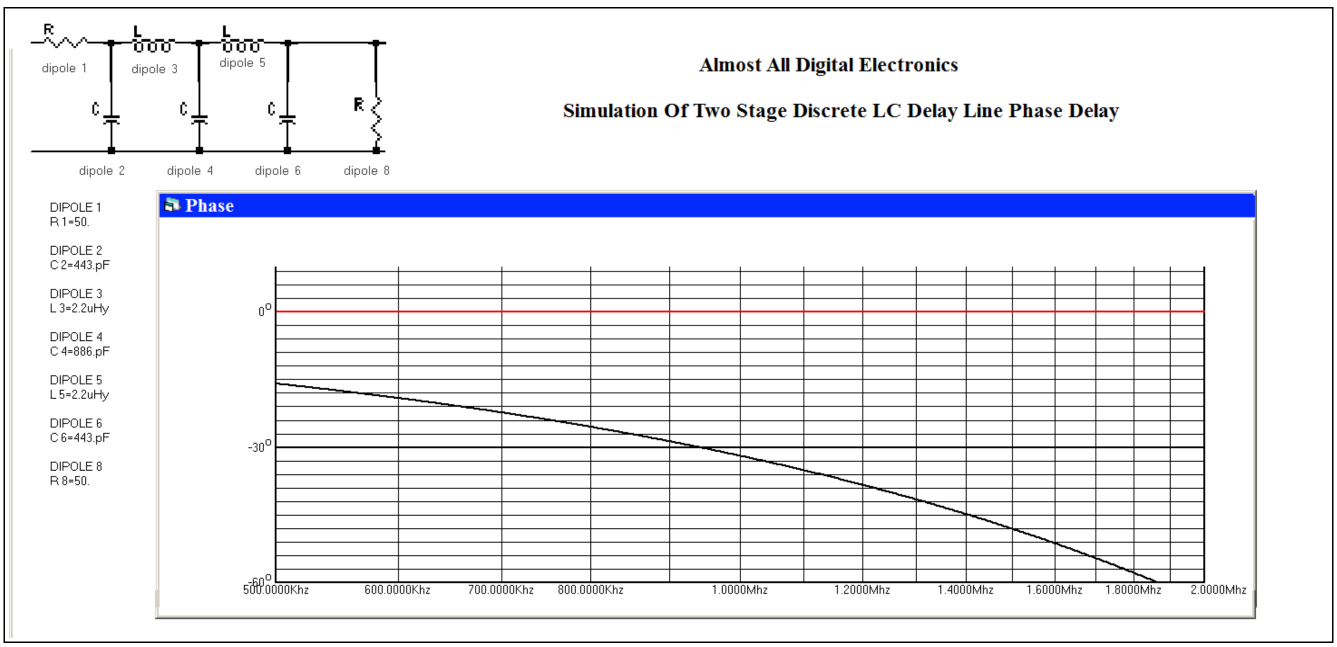
When you open the AADE program, there are a number of options at the top of the window. The DESIGN and ANALYZE options are the ones that I use most often. When you left click on DESIGN, you can select the type of filter you want, namely Butterworth, Chebyshev, etc. (and then select LOW PASS, HIGH PASS, BAND PASS, BAND REJECT), select thee order (number of stages), modify the filter in various ways by removing or adding components, and change the values of the components by left clicking on the components of the schematic. For the discrete LC delay circuit at the beginning of this article I use Chebyshev and low pass, and then order 3 (the default is 5) when the next window opens. After clicking through several more windows, the schematic appears and the component values can be changed. When you left click on ANALYZE you can select Phase, Input Impedance, Output Impedance, Voltage Effective Gain, and a number of other options. When one of those options is selected, you can then select the frequency range and other ranges, like degree range for the phase simulation.

An AADE phase simulation of the discrete LC delay circuit given near the beginning of this article is shown below. The LC delay circuit has a constant 88.3 nS delay, but the degree delay is not constant. To convert time to degree delay at a particular frequency, say 1 MHz, do the following. 1 MHz is 10^6 cycles/sec, or 1/10^6 sec/cycle, or 10^9/10^6 nS/cycle, or 10^3 nS/cycle, or 1000/360 nS/degree, or 0.36 degree/nS. Thus at 1 MHz the 88.3 nS delay is (0.36)(88.3) degrees = 31.8 degrees. In view of the previous, the phase delay of 88.3 nS can be converted to degree delay at other frequencies by simple ratios. For example, at 500 kHz the degree delay is (0.5)(31.8) = 15.9 degrees, and at 1.6 MHz (1.6)(31.8) = 50.9 degrees. As can be seen below, according to the AADE simulation, the discrete LC delay circuit delay is very accurate at 0.5 MHz and 1.0 MHz, but about 2 degrees off at 1.6 MHz.



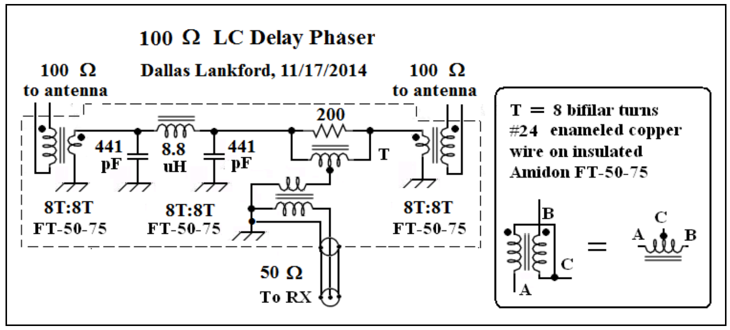
This inaccuracy at 1.6 MHz intrigued me, and as a consequence I decided to simulate a two stage discrete LC delay circuit with 44.15 nS time delay per stage. So below is an AADE phase delay simulation of two discrete LC delay stages of 44.15 nS delay. The AADE filter was constructed similar to the one stage filter above.

As can be seen below, the phase of the two stage discrete LC delay line is very accurate up to 1.6 MHz.



Should I replace my single stage discrete LC delay circuits with two stage discrete LC delay circuits? I think not. I did EZNEC pattern simulations at 1.6 MHz with the original phases and with the original phases advanced by 2 degrees and found no observable difference in the two patterns or two gains.

It easy to design discrete LC delay lines for other input and output impedances. I designed the phasers for my Quoddy Head 2011 DXpedition with 100 ohm input and output discrete delay lines. Their schematic is given below at right. If you look at the formulas for the discrete LC delay circuits near the beginning of this article you will see that by doubling the inductor and halving the capacitors values the input and output impedance is doubled while the time delay remains the same. Note that the 100 ohm resistor of the magic T combiner must be changed to 200 ohms. I do not recall why I decided to change the input and output impedances of the discrete delay line.

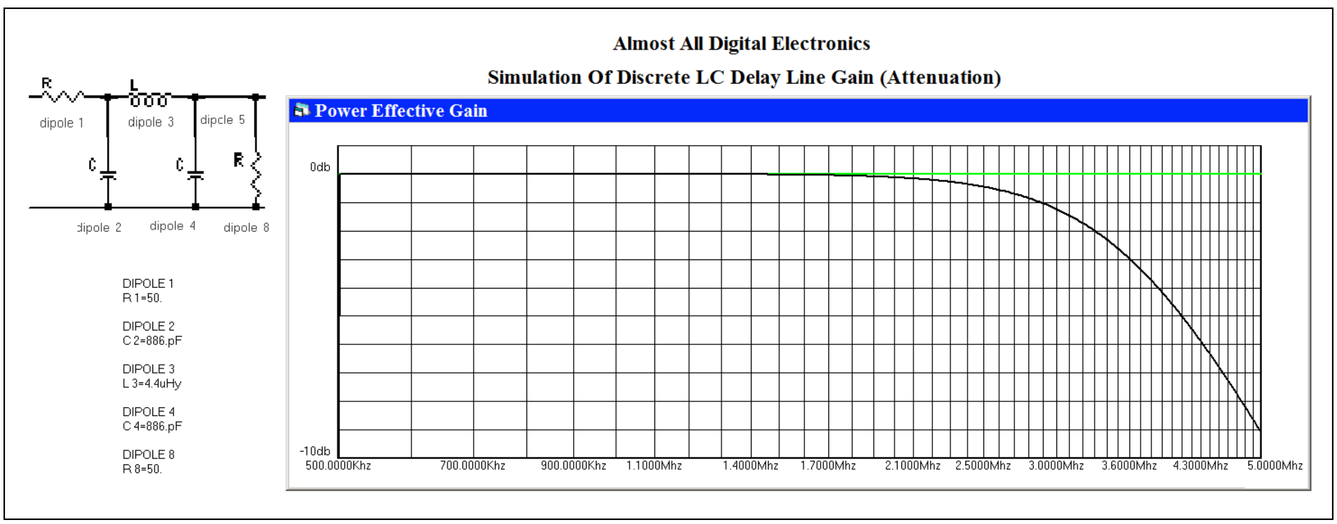


The delay time of the discrete LC delay line can be changed by increasing the values of the inductor and capacitors by the same amount. This would be done if one desired greater separation between the centers of the antennas. For an increase in separation by a factor of x, the values of L and C are each multiplied by x. For example, if a separation of 120 feet between the centers of the antennas is used, the the values of L and C should each be multiplied by 1.2. In the case of the 50 ohm discrete LC delay line with C = 883 pF and L = 4.4 µH, for 120 feet separation between the two antenna centers C = 1060 pF and L = 5.3 µH. The change 1060 pF is easy to approximate with 1000//62, and the 5.3 µH could be approximated with two 2.2 µH and a 1.0 µH in series. I can't think of any reason for 120 feet of separation, but merely gave this example to illustrate how discrete LC delay lines can be made for separations other than 100 feet.

The attenuation of the single stage discrete LC delay lines discussed above is virtually nil throughout the MW band. An AADE simulation of "power effective gain" (attenuation) of these delay lines is given below. Roll off starts ever so slightly around 1500 kHz. The amount of attenuation at 1600 kHz is clearly less than a tenth of a dB.

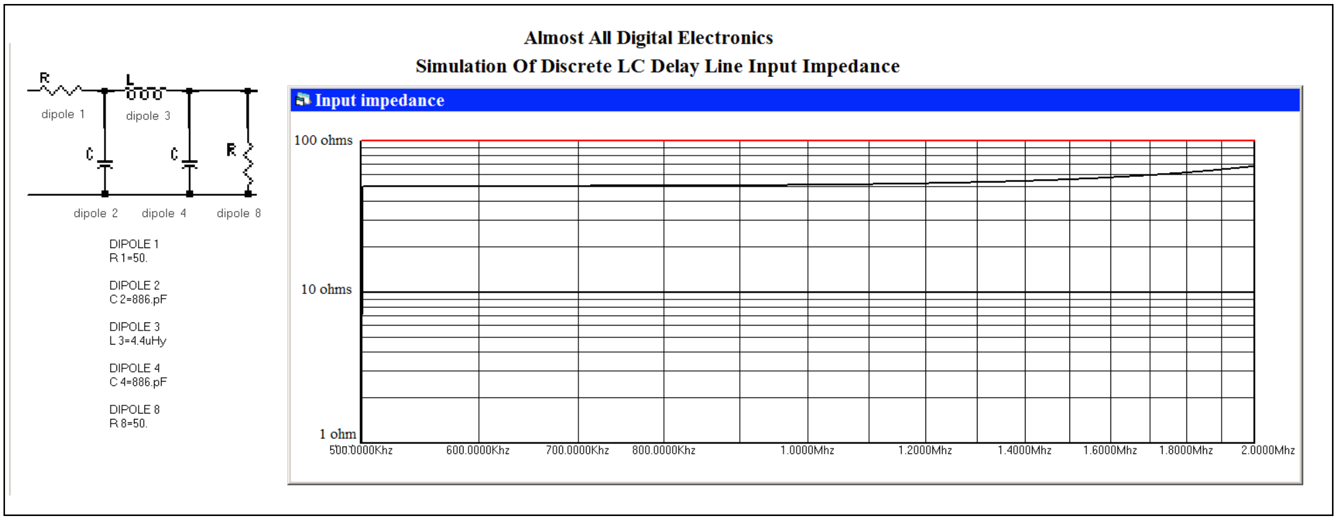
The attenuation of the dual stage discrete LC delay line discussed above is nil throughout the MW band; its attenuation begins to roll off about 2700 kHz. This AADE attenuation simulation is not shown here.

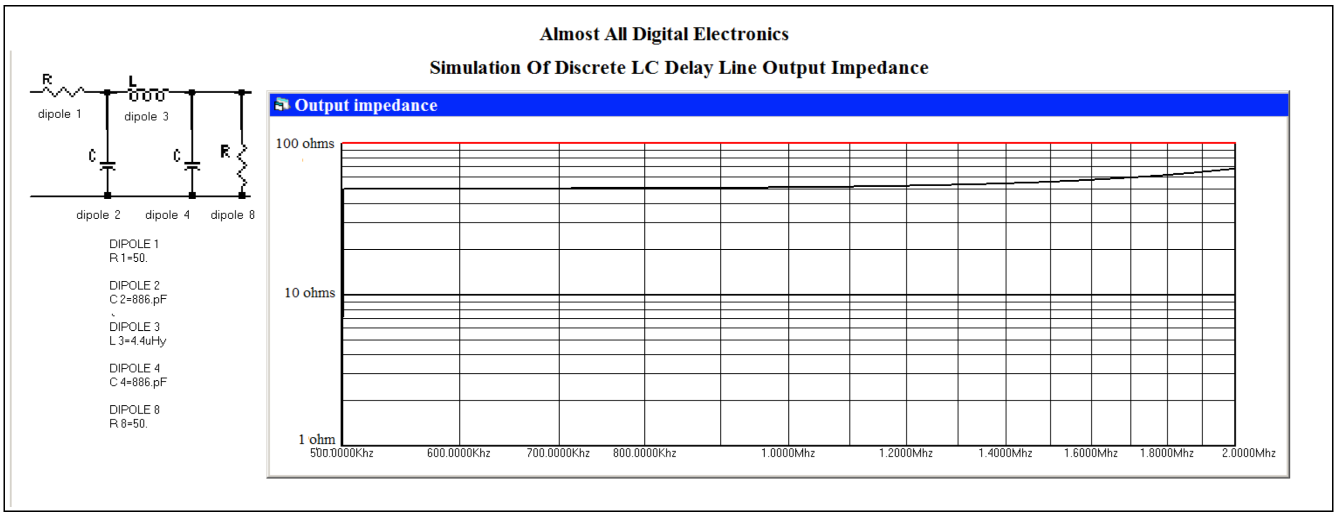
Should I replace the single stage discrete LC delay lines in my phasers with dual stage delay lines? Nope. EZNEC simulation shows that there is no difference in the patterns at 1.6 MHz of the arrays I have used (QDFA, Q95, dual delta flag array) when 0.1 dB attenuation due to the discrete LC delay lines is included.



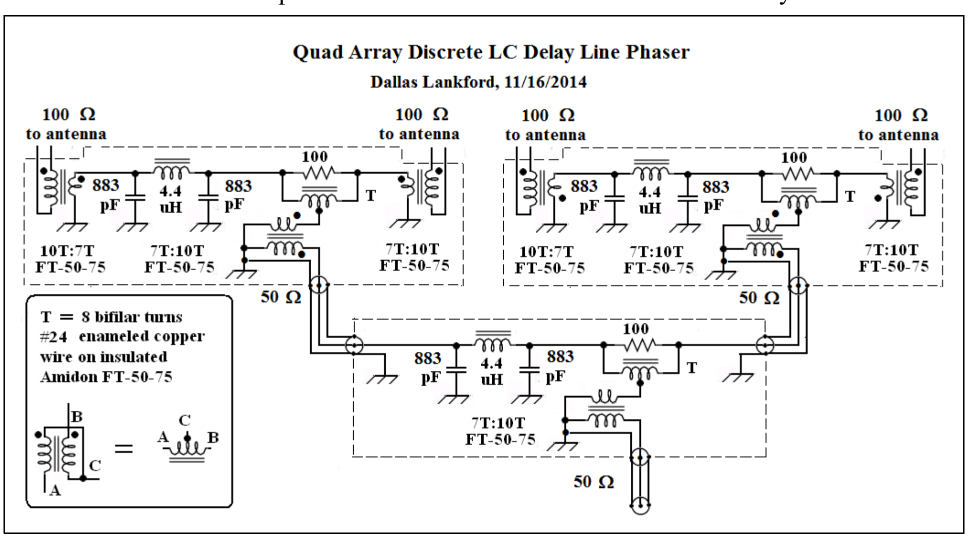
The Almost All Digital Electronics (free!) filter simulation software has been an essential part of my analyses of discrete LC delay lines. Unfortunately, the filter software is currently unavailable because AADE has been shut down due to serious illness of the owner

AADE simulations (on the next page below) of the input and output impedance shows that they are both 50 ohms in the lower MW band, but begin to rise slowly at mid band until they reach 60 ohms at 1600 kHz. Is this a problem? No. Calculation of the mismatch using an online Mismatch Calculator shows that the mismatch at the input and output of the discrete LC delay line is 0.036 ohms each, for a total of 0.072 ohms. EZNEC simulation of the patterns and gains for the antennas I use (dual delta flag array and QDFA) show that there is no observable difference in the patterns and gains with the attenuation included in the delay signal path compared to the patterns and gains with no loss. Even at 2 MHz where the input and output impedances are 70 ohms, there are no observable differences in the patterns and gains. To double check these results a second online Mismatch Calculator got the same mismatch loss as with the first Mismatch Calculator.





All of the previous examples have dealt with phasers for dual antenna systems. Below is a discrete LC delay line phaser for quad arrays.. It consists of three components. Two components are discrete LC delay line phasers like the one described earlier above in this article. The third component is like the first two except that is is not designed for 100 ohm twin lead input but for 50 ohm coax. The third component could be used with a dual antenna array which has 50 ohm coax lead in.

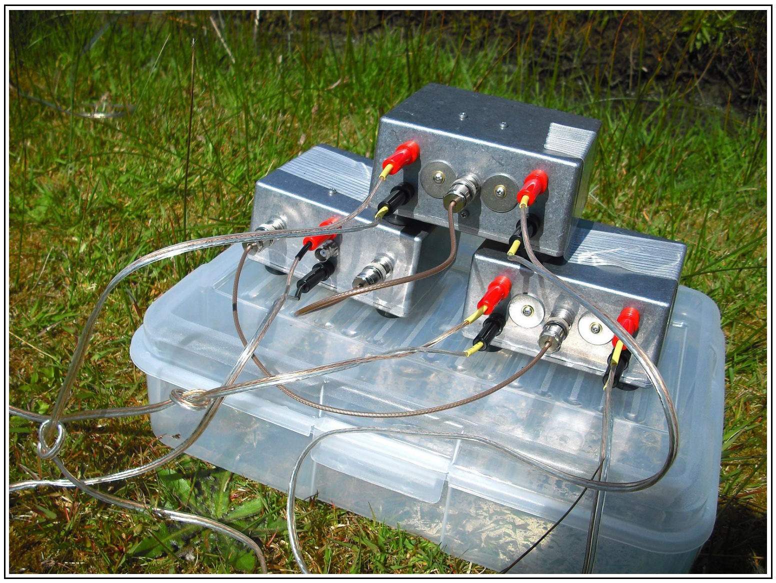


But it is not. It is used to phase the two dual arrays which are connected to the first two phasers.

I have not mentioned this before, but is is essential that the right hand sides of the 100 ohm twin lead be connected to the “hot” sides of the antennas. Otherwise the dual array phasers will not generate the wide null apertures the dual arrays are capable of. The reason for this is that the two antennas of each dual array are connected to the phasers 180 degrees out of phase if, and only if, the twin leads left hand sides are connected to the “hot” sides of the antennas. It is also important that the transformers be connected as shown by the phasing dots on the transformer windings. Again, the dual arrays will not have wide null apertures if that is not done. The same is true for qad arrays.

Also, and I have not mentioned this before: **ALL ANTENNA LEAD INS SHOULD BE EQUAL LENGTHS** for the antenna arrays and phasers discussed in this article. Different length lead ins wold have different delays and degrade the array patterns.

As you may have guessed by looking at the diagram of the quad phaser above, my basic idea for a quad array was to take two dual arrays with very good patterns, separate them by some distance (I took 200' between the centers of the arrays), double the time delay (the delay distance between the two arrays was double the delay distance between the antennas of the dual arrays), and do EZNEC simulations. Curiously, the 30 dB null aperture of the quad flag array was not much better than the 30 dB null aperture of a dual flag array.   So I started “tinkering”, which is easy to do with EZNEC. I quickly found that the pattern improved as the delay between the dual arrays was decreased. But I also found that if the delay between the two dual arrays was made too small, the the gain decreased and the pattern degraded. Using the same delay as a single dual array for the two dual arrays seemed like a good compromise, so that is what I did.



The Quad Array Discrete LC Delay Line Phaser is basically the quad phaser that I used at Grayland in 2009; see the photo at right. There is one minor difference. The output of the phaser at right is 100 ohm twin lead. Note that I used 18 gauge speaker wire for my 100 ohm twin lead. It seems to work about as well as the much more expensive 100 ohm twinax.

When very long lead ins are required to connect the phaser with the receiver, as was the case at Grayland 2009, and isolating amplifier is required between the output of the phaser and the very long lead in.   See my article “Phased Delta Flag Arrays” for additional information on this problem.

A similar quad phaser with three components was used at Quoddy Head 2011.   The discrete LC delay lines used in the Quoddy Head phasers were 100 ohm delay lines.

Perhaps (?) I should also say the following: **ALL ANTENNAS SHOULD BE IDENTICAL** for the antenna arrays and phasers discussed in this article. If two antennas were different sizes (or shapes, or types), then their output amplitudes would be different, and when they were combined after phase shifting the amplitudes 180 degrees, the signals would not completely cancel, and a null wold not be created. Cancellation (nulling) of two signals requires that they have identical amplitudes and 180 degree phase difference.

Additional information about discrete LC delay line phasers is contained in my articles about my DXpeditions (Quoddy Head 2008 and 2011, and Grayland 2009), and my articles about my invention and development of phased flag arrays and phased delta flag arrays. These are available in my Yahoo group thedallasfiles2. The URL for the dallasfiles2 is the following: groups.yahoo.com/neo/groups/thedallasfiles2 .